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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,028	10/14/2003	Andrej Kocev	200208956-1	4863

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EXAMINER	
BROWN, MICHAEL J	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/685,028	KOCEV ET AL.	
	Examiner	Art Unit	
	Michael J. Brown	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) *19-36* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/14/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 10/14/2003 was filed. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Harrell(US Patent 5,682,554).

As to claim 1, Harrell discloses a system(computer system 20, see Fig. 2), comprising a timing logic unit(interface 23, see Fig. 2) coupled to produce a predetermined number of pulses(PRESET VALUE, see Fig. 2) in response to a transaction request(INTERRUPT_HC, see Fig. 2) transmitted from a source device(host computer 22, see Fig. 2) to a target device(graphics processor 21, see Fig. 2), wherein the timing logic unit is configured to generate a time expired signal(ALMOST_FULL, see Fig. 2) upon producing a last one of the predetermined number of pulses(PRESET VALUE, see Fig. 2). Harrell also discloses a processor(FIFO 24, see Fig. 2) for executing program instructions(DATA, see Fig. 2) configured to programmably alter a

rate(data transfer rates, see column 4, line 44) at which the predetermined number of pulses are produced by the timing logic unit, thereby adjusting an expiration period for completing a transaction cycle(CYCLE_STALL_HC, see Fig. 2) associated with the transaction request.

As to claim 2, Harrell discloses the system wherein the program instructions are configured to programmably decrease the rate for increasing the expiration period(see column 8, lines 5-19).

As to claim 3, Harrell discloses the system wherein the program instructions are configured to programmably increase the rate for decreasing the expiration period(see column 8, lines 5-19).

As to claim 4, Harrell discloses the system wherein the timing logic unit is arranged within at least one of the source and target devices(see column 4, line 66-column 5, line 6; and column 14, lines 4-11).

As to claim 5, Harrell discloses the system further comprising a carrier medium(lines 41 and 43, see Fig. 2) configured to transfer information associated with the transaction cycle between the source device and the target device.

As to claim 6, Harrell discloses the system wherein the carrier medium comprises one or more buses within a computer system, such that the source and target devices are each arranged within the computer system(see column 6, lines 10-11 and lines 31-32).

As to claim 7, Harrell discloses the system wherein the carrier medium comprises a wired or wireless network interface for coupling the system to one or more additional

systems, such that the source device is arranged within the system and the target device is arranged within one of the additional systems, or vice versa(see column 6, lines 10-11 and lines 31-32).

As to claim 8, Harrell discloses a computer system(computer system 20, see Fig. 2), comprising a source device(host computer 22, see Fig. 2) configured to initiate a transaction cycle(OUT_CLK, see Fig. 2) by sending a transaction request(INTERRUPT_HC, see Fig. 2) to a target device(graphics processor 21, see Fig. 2); a timing logic unit(interface 23, see Fig. 2) arranged within the target device, wherein the timing logic unit comprises a time register(register 27, see Fig. 2) for storing a predetermined expiration value(PRESET VALUE, see Fig. 2). Harrell also discloses a first counter(down counter 25, see Fig. 2) for receiving a number of pulses corresponding to the predetermined expiration value, and generating a time expired signal(ALMOST_FULL, see Fig. 2) upon receipt of a last one of the number of pulses(PRESET VALUE, see Fig. 2). Harrell further discloses a memory device(FIFO 24, see Fig. 2) for storing program instructions(DATA, see Fig. 2) configured to programmably alter a rate(data transfer rates, see column 4, line 44) at which the number of pulses are received by the first counter, thereby adjusting an expiration period for completing the transaction cycle(CYCLE_STALL_HC, see Fig. 2).

As to claim 9, Harrell discloses the computer system wherein the program instructions are configured to programmably decrease the rate, thereby increasing the expiration period, if a target-ready signal(clock signal OUT_CLK, see Fig. 2) is not asserted by the target device before the time expired signal is generated by the timing

logic unit.

As to claim 10, Harrell discloses the computer system wherein the program instructions are configured to programmably increase the rate, thereby decreasing the expiration period, if a target-ready signal(clock signal OUT_CLK, see Fig. 2) and a source-ready signal(clock signal IN_CLK, see Fig. 2) are asserted by the target device and the source device, respectively, before the time expired signal is generated by the timing logic unit.

As to claim 11, Harrell discloses the computer system wherein the target-ready signal is asserted upon completion of the transaction request by the target device, and wherein the source-ready signal is asserted when the source device is ready to send or receive transaction data, which corresponds to the transaction request, for completing the transaction cycle(see column 5, lines 9-15 and lines 20-25).

As to claim 12, Harrell discloses the computer system wherein the target-ready signal is asserted upon completion of the transaction request by the target device, and wherein the source-ready signal is asserted when the source device is ready to send or receive transaction data, which corresponds to the transaction request, for completing the transaction cycle(see column 5, lines 9-15 and lines 20-25).

As to claim 13, Harrell discloses the computer system further comprising a processor coupled for receiving interrupt signals from a clock source at a fixed rate and for executing the program instructions in response to the interrupt signals(see column 6, lines 18-25 and lines 39-46).

As to claim 14, Harrell discloses the computer system wherein the timing logic

unit further comprises a control register(register 28, see Fig. 2) for storing an enable signal, a second counter(down counter 26, see Fig. 2) for generating the number of pulses, and a circuit(interface 23, see Fig. 2) comprising the time register and the first counter, wherein the circuit is coupled to receive the enable signal and at least one of the number of pulses every nth time the processor receives an interrupt signal, wherein `n` is a programmable value selected from a group consisting of any positive, non-zero integer value.

As to claim 15, Harrell discloses the computer system further comprising a primary bus bridge logic unit(lines 40 and 42, see Fig. 2) configured to coordinate transactions between the processor, the memory device, and one or more peripheral devices coupled to the primary bus bridge logic unit over one or more peripheral buses of the computer system.

As to claim 16, Harrell discloses the computer system wherein the timing logic unit is arranged within the primary bus bridge logic unit(see column 4, line 66- column 5, line 6).

As to claim 17, Harrell discloses the computer system wherein the timing logic unit is arranged within the one or more peripheral devices(see column 4, line 66-column 5, line 6; and column 14, lines 4-11).

As to claim 18, Harrell discloses the computer system further comprising a secondary bus bridge unit coupled to the primary bus bridge unit(lines 40 and 42, see Fig. 2) over one of the peripheral buses and having one or more additional peripheral

devices coupled thereto, wherein the timing logic unit is arranged within the secondary bus bridge unit and/or within the one or more additional peripheral devices.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Brown whose telephone number is (571)272-5932. The examiner can normally be reached on Monday-Friday from 7:00am to 3:30pm(EST).

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIRS) system. Status information for the published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications are available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 886-217-9197 (toll-free).

Michael J. Brown
Art Unit 2116

THUAN N. DU
PRIMARY EXAMINER